WHAT IS CLAIMED IS

1. A method for identifying design errors in an integrated circuit comprising:

inferentially comparing current design information to historical design information; and

detecting at least one probable root cause of at least one design error using the inferential comparison of current and historical design information.

2. The method of claim 1 wherein inferentially comparing current design information to historical design information comprises performing a probabilistic comparison of the current design information and the historical design information and inferring probabilistic relationships between the current and historical design information.

3. The method of claim 1 wherein the at least one design error is predicted by an inference engine based on the inferential comparison of the current design information and the historical design information.

4. The method of claim 1 wherein an inference engine infers the at least one design error by observing an anomalous design state.

5. The method of claim 1 wherein the current design information includes design tasks, design conditions and the at least one design error.

6. The method of claim 5 wherein a probabilistic model generates a set of conditional probabilistic dependencies between the design tasks, the design conditions and the at least one design error.

7. The method of claim 1 wherein detecting the at least one probable root cause of the at least one design error further comprises generating and using a probabilistic model to update conditional probabilistic dependencies between design tasks and design conditions probabilistically associated with the at least one design error.

8. The method of claim 7 wherein an inference engine analyzes the conditional probabilistic dependencies between design tasks and design conditions and the at least one design error in combination with the historical design information to infer the at least one probable root cause of the at least one design error.

9. The method of claim 1 wherein at least one error case is generated for each of the at least one design errors.

10. The method of claim 9 wherein at least one probabilistic match is inferred between the at least one error case and historical design state information associated with design errors included in the historical design information.

11. The method of claim 10 wherein the at least one probabilistic match indicates the at least one probable root cause of the at least one design error.

12. The method of claim 11 wherein current and historical design information probabilistically associated with the at least one probabilistic match is presented in an interactive computer program environment.

13. The method of claim 1 wherein an alert is automatically generated when the at least one probable root cause of the at least one design error is detected.

14. The method of claim 1 wherein the current design information includes any of:

current information and data delimiting current design attributes;

design verification and simulation test results for the current design;

current design states;

tools used to develop the current design;

tasks completed in the current design; and

conditions existing in the current design.

15. The method of claim 1 wherein the historical design information includes any of:

errors that have occurred in previous designs;

design tasks associated with the errors that have occurred in previous designs;

design tools associated with the errors that have occurred in previous designs;

design conditions associated with the errors that have occurred in previous designs; and

solutions used to address the errors that have occurred in previous designs.

16. A system for determining a current design state of an integrated circuit design, comprising:

an inference engine for automatically inferring at least one source of at least one design error in the circuit design;

a probabilistic model for determining conditional relationships between the at least one design error, and attributes of the current design having probabilistic relationships to the at least one design error; and

a dynamic data matrix comprising current design information, the conditional relationships between the at least one design error, and the attributes of the current design having the probabilistic relationships to the at least one design error.

17. The system of claim 16 wherein the inference engine uses inferential reasoning to compare current design information to historical design information compiled from prior integrated circuit designs to identify probabilistic relationships between the current design information and the historical design information.

18. The system of claim 17 wherein the inference engine infers the source of the at least one design error using the probabilistic relationships between the current design information and the historical design information.

19. The system of claim 16 wherein the dynamic data matrix further comprises design tasks, design conditions, predicted and detected design errors, and conditional probabilities associated with interrelationships between the tasks, conditions, and predicted and detected design errors.

20. The system of claim 16 wherein the dynamic data matrix is automatically presented in an interactive computer program environment.

21. The system of claim 16 wherein the inference engine is automatically presented in an interactive computer program environment.

22. A computer-readable medium having computer-executable modules for identifying at least one design error in an integrated circuit design comprising an inference processor that automatically infers at least one probabilistic source of the at least one design error.

23. The computer-readable medium of claim 22 further comprising a probabilistic model processor for automatically determining conditional probabilistic relationships between the at least one design error of the current design, and design attributes probabilistically associated with the at least one design error.

24. The computer-readable medium of claim 23 further comprising a data processor for dynamically generating and displaying current design information, the conditional probabilistic relationships between the at least one design error of the current design, and design attributes probabilistically associated with the at least one design error, in an interactive computer program environment.

25. The computer-readable medium of claim 22 wherein the inference processor automatically uses inferential reasoning to compare current design information to historical design information compiled from prior integrated circuit designs.

26. The computer-readable medium of claim 25 wherein the inference processor identifies conditional probabilistic relationships

between the current design information and the historical design information.

27. The computer-readable medium of claim 24 wherein the probabilistic model processor is initialized using data from the data processor.

28. The computer-readable medium of claim 22 wherein an alert processor automatically generates an alert when the inference processor infers the at least one probabilistic source of the at least one design error.

29. The computer-readable medium of claim 22 wherein the inference processor is presented in an interactive computer program environment.